IN THE SPECIFICATION:

Please replace the paragraph appearing on page 1, lines 6-26 of the specification with the following amended paragraph:

-- The present invention is related to commonly assigned and co-pending U.S. Patent Applications [[_____]] 09/671/876, filed September 28, 2000, (Attorney Docket No. AUS9-2000-0569) entitled "APPARATUS AND METHODS FOR IMPROVED DEVIRTUALIZATION OF METHOD CALLS", [[_____]] 09/671,770, filed September 28, 2000, (Attorney Docket No. AUS9-2000-0570) entitled "APPARATUS AND METHOD FOR AVOIDING DEADLOCKS IN A MULTITHREADED ENVIRONMENT", [[_____]] 09/671,973, filed September 28, 2000, (Attorney Docket No. AUS9-2000-0572) entitled "APPARATUS AND METHOD FOR IMPLEMENTING SWITCH INSTRUCTIONS IN AN IA64 ARCHITECTURE", [[_____]] 09/671,877, filed September 28, 2000, (Attorney Docket No. AUS9-2000-0573) entitled "APPARATUS AND METHOD FOR DETECTING AND HANDLING EXCEPTIONS", [[_____]] 09/671,771, filed September 28, 2000, (Attorney Docket No. AUS9-2000-0584) entitled "APPARATUS AND METHOD FOR VIRTUAL REGISTER MANAGEMENT USING PARTIAL DATA FLOW ANALYSIS FOR JUST-IN-TIME COMPILATION", [[_____]] 09/671,873, filed September 28, 2000, (Attorney Docket No. AUS9-2000-0585) entitled "APPARATUS AND METHOD FOR AN ENHANCED INTEGER DIVIDE IN AN IA64 ARCHITECTURE", and [[_____]] 09/671,874, filed September 28, 2000, (Attorney Docket No. AUS9-2000-0586) entitled "APPARATUS AND METHOD FOR CREATING INSTRUCTION GROUPS FOR EXPLICITLY PARALLEL ARCHITECTURES", filed on even date herewith and hereby incorporated by reference. --

Please replace the paragraph appearing on page 7, lines 9-24 of the specification with the following amended paragraph:

-- The present invention provides an apparatus and method for creating instruction bundles for explicitly parallel architectures. In particular, the present invention provides an apparatus and method for creating instruction bundles for implementations of the IA64 explicitly parallel architecture. The IA64 architecture is described in the "Intel IA-64 Architecture Software Developer's Manual" ~~available for download from http://developer.intel.com/design/Ia-64/downloads/24531702s.htm~~, which is hereby incorporated by reference. While the present invention will be described with reference to the Itanium implementation of the IA64 architecture, the present invention is not limited to such. Rather, the present invention is applicable to any explicitly parallel architecture and any implementation of the IA64 architecture in particular. --

Please replace the paragraphs starting on page 11, line 15 to page 12, lines 20 of the specification with the following amended paragraphs:

-- The present invention provides a mechanism to quickly organize instructions into valid bundles that will efficiently exploit the resources of the target processor. With the present invention, bundle creation is the final step in compilation and the bundles are emitted, i.e. code is generated for the instructions, directly into a code buffer associated with the processor. The input to the bundle creation is a stream of intermediate instructions organized into instruction groups by a previous operation. The step of organizing intermediate instructions into instruction groups may be performed, for example, using the apparatus and method described in co-pending and commonly assigned U.S. Patent Application Serial No. [[_____]] 09/671,874, filed September 28, 2000, (Attorney Docket No. AUS9-2000-0586-US1), which is hereby incorporated by reference. It is assumed that the creator of the instruction groups is aware of the limitations and special requirements of the target implementation and that the instruction groups will not include instruction combinations that will force oversubscription of hardware resources assuming optimal bundling is performed. The end of each instruction group is identified by a stop flag set to one in the final intermediate instruction of each instruction group.

With the present invention, prior to performing the instruction bundle creation, the apparatus and method of the present invention gathers information about the underlying architecture for use in the instruction bundle creation. The information gathered includes the number of each type of execution unit available and the number of bundles that can be dispatched concurrently by the architecture. For example, Itanium has two I-units, two M-units, two F-units, and three B-units and can dispatch a maximum of two bundles concurrently. As described in the incorporated U.S. Patent Application Serial No. [[_____]] 09/671,874, filed September 28, 2000, (Attorney Docket No. AUS9-2000-0586-US1), this information may be obtained as part of or previous to the step of instruction group creation. --